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In re the application of
  Whetsel   TI-14124D.6

Application No. 10/691,225   Art Unit: 2133

Filed: 10/22/2003   Examiner: Britt, Cynthia

Title: Circuit With Expected Data Memory Coupled to Serial Input
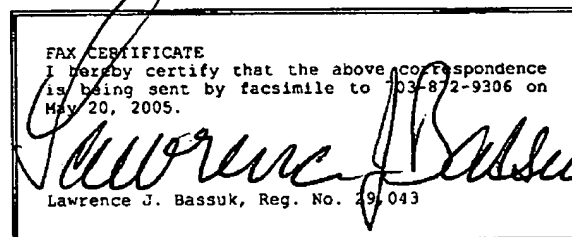Lead

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Information Disclosure Statement B
US Patents and Applications and Foreign Patent

May 20, 2005

FAX CERTIFICATE
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Lawrence J. Bassuk, Reg. No. 29,043

Asst. Commissioner for Patents
P.O. Box 1450
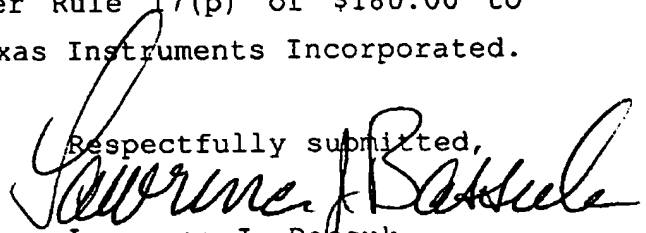Alexandria, VA   22313-1450

Dear Sir:

Applicant requests consideration of all US patents and
patent publications and a foreign patent listed on enclosed form
PTO-1449B. Applicant includes only a copy of the foreign patent
document.

Under Rule 97(h), the filing of this information disclosure
statement shall not be construed to be an admission that the
information cited in this statement is, or is considered to be
material to patentability as defined in Rule 56(b).

Applicant points out particular references and figure
numbers and provides a brief explanation of each cited reference
in Attachment A.

Please consider this statement as being filed under Rule 97(c), after the period specified in Rule 97(b), but before the mailing date of either a final action, or a notice of allowance. Under Rule 97(c), applicant submits the fee set forth in Rule 17(p). Please charge the fee under Rule 17(p) of $180.00 to Deposit Account Number 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5458

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Attachment A

In the following, a brief description may contain a statement that the patent corresponds to one or more other patents. No description of the corresponding patents is provided to avoid duplicating a description of the same disclosure.

The described patent may be a divisional of or a continuation-in-part of the corresponding patent. A corresponding patent may be a divisional of the described patent. A corresponding patent may have issued from one of plural applications that appear to have the same drawing figures and were filed on the same day as the described patent. A corresponding patent may be a foreign patent claiming priority from the described patent or it may be a foreign patent providing priority for the described patent.

US Patent Documents

Re. 31,056 to Chau et al. discloses a high speed testing circuit 10 coupled between a test system computer 12 and a device under test 14. The circuit 10 supplies stimuli signals, receives output signals, and provides parametric testing. Reissue of US 4,092,589.

US 3,633,100 to Heilweil, et al., discloses applying two binary levels and an intermediate level of inputs to binary logic under test and to simulation logic. The outputs of the circuit under test and the simulation logic are compared to ascertain a good circuit

US 3,651,315 to Collins discloses a digital inspection system. The outputs from a product under test are compared with the outputs of a known good unit.

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US 3,657,527 to Kassabgi, et al., discloses a system for automatically checking boards bearing integrated circuits. A program card is read automatically to provide both test input signals to the board and simulation output signals representative of the correct output signals.

US 3,723,868 to Foster discloses digitally counting predetermined numbers of clock pulses during preselected timing intervals to determine the precise time interval between distinct edges of the output from a circuit under test and provide a GO/NO-GO indication.

US 3,739,193 to Pryor discloses a feedback network where the feedback signal is sufficiently small to be overridden by the input signal.

US 3,789,359 to Clark, Jr., et al. discloses a synchronism indicator for a convolutional decoder.

US 3,824,678 to Harris, et al. discloses a process for laser scribing beam lead semiconductor wafers.

US 3,826,909 to Ivashin discloses a binary counter applying identical signals to a tested and standard reference circuit. Output indicators display any difference between the tested and standard reference circuit.

US 3,831,149 to Job discloses a control device having presettable control elements, one for each test lead, each presettable to a desired state for specifying signal-combinations to be monitored. The signal-combinations control the read-in and/or read-out of information from a memory.

US 3,838,264 to Maker discloses a device for checking the contents of a store of a computer that is normally under control of a chain of timing pulses and an address register. The device

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includes a switching device that sums a quantity of the timing pulses and compares the sum to a known quantity.

US 3,873,818 to Barnard discloses reducing the size of a random access memory storing test patterns. Similar test words are stored as an initial word with indications and binary reconstruction means for generating the other similar test words.

US 3,976,940 to Chau et al. discloses a test circuit 10 including a pair of comparator circuits, each of which is disposed for comparing two minimum threshold amplitudes of responses from a device under test. A multiplexer switches the outputs of the two multiplexers to the device under test.

US 4,023,142 to Woessner discloses a common reliability and service bus connected to each functional unit of LSI apparatus. The bus provides for an addressed unit to go through an operation after a test pattern has been loaded into the unit while the system continues to operate concurrently. Figure 4 depicts a control system adapter 200 with shift register configuration 210. Data bits 0-7 appear to be loaded in parallel into Diagnostic Address Register 175, Mode Register 1 120, Mode Register 2 180, Mode Register 3 185, and Shift Register 170. Level Shifting Serial Design latches 210 form a scan path. An exclusive OR circuit 400 compares the data from shift register 210 to be compared serially, bit-by-bit, with an expected data pattern loaded into register 170.

US 4,066,882 to Esposito discloses an automatic computer controlled digital test device that tests circuits by other than random test techniques. The device relies upon software test generation techniques and test programs written in high level test languages and stored on a magnetic disk.

US 4,086,375 to LaChapelle, Jr., et al. discloses a batch process providing beam leads for microelectronic devices having metallized contact pads.

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US 4,092,589 to Chau et al. Same disclosure as Re. 31,056.

US 4,092,733 to Coontz, et al. discloses an electrically alterable, non-volatile interconnect that selectively connects and disconnects microcircuit elements formed on a wafer. Corresponds to JP 52-136,534.

US 4,108,359 to Proto discloses a device for detecting errors in the execution of a sequence of coded instructions. A feed-back shift register generates a digital sequence combined with the sequence of instructions to compute a unique sequence check word that is compared to a stored, known good check word.

US 4,146,835 to Chnapko et al. discloses a method of testing the difference in propagation delays through gate circuits of an integrated circuit. The method generates a reference signal at the sensing of the first output of one of the gate circuits and adding a maximum delay time. Any actual signal occurring after the end of the maximum delay time indicates a delay beyond specification.

US 4,161,276 to Sacher, et al. discloses comparing transitions and final logical states of a known good part with a part under test.

US 4,216,539 to Raymond, et al. discloses a programmed processor controlling a set of switches to apply a test signal to a selected node and connect the response from that node to a functional tester.

US 4,242,751 to Henckels, et al. discloses peripherally probing circuit boards and the like with insights into predictable or likely failures and over-riding or discontinuing normal computer back-tracking.

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US 4,264,807 to Moen, et al. discloses an electric counter including a pair of counter segments connected in cascade. The counters count in Gray code. The second counter segment increments upon the first segment changing from 10 to 00. Corresponds to EP 0,017,091 and JP 55-135,424.

US 4,268,902 to Berglund, et al. discloses a maintenance interface for interfacing a service processor and a central processor operating synchronously to each other. The interface circuitry synchronizes the service processor to the central processing unit and decodes commands from the service processor. The interface circuitry also establishes communication from the central processing unit to the service processor and resolves communication contention between the processors.

Circuitry provides independent control of the clocks to each functional unit or shift ring (scan path) and the functional unit interface signals to other functional units or arrays. The interface includes a Level Sensitive Scan Design (LSSD) testing system with four separate shift rings and provides degating of central processing unit interfaces as required for this testing approach.

US 4,286,173 to Oka, et al. discloses a logical circuit having bypass for testing logical circuits. Corresponds to JP 54-127,245.

US 4,308,616 to Timoc discloses simulating a fault on a selected connection with the output of a shift register in a digital network.

US 4,309,767 to Andow, et al. discloses a monitor system judging the operating condition of an A-D converter from the contents of an adder.

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US 4,312,066 to Bantz, et al. discloses an interface between a host processor and a diagnostic/debugging processor that troubleshoots the hardware and software of the host processor. The host uses the Level Sensitive Scan Design rules.

The disclosed system allows the machine state and memory of the Host CPU to be captured at the end of an instruction or at the end of a cycle. It further allows selective reading and writing of the memory state by conditioning the H-machine with state information that will cause words from or to memory to be transferred to the D-machine. The system allows control over interruption, channel activity and address translation and provides a diagnostic CPU with its own memory to perform diagnostic and debug functions.

US 4,339,710 to Hapke discloses a MOS integrated circuit using field effect transistors including a circuit arrangement for rapidly testing various blocks of the circuit.

US 4,357,703 to Van Brunt discloses performing dynamic testing of complex logic modules at full system clock rates and is resident on each LSI chip under test. The test system includes transmission gates to alter logic paths, and an associated test generator and accumulator at each of the test input and test output.

US 4,365,334 to Smith, et al. discloses producing final test data in response to a stored Logic List for each logic circuit type and stored connection information for a logic circuit under test.

US 4,366,478 to Masuda, et al. discloses a general purpose signal transmitting and receiving apparatus for transmitting and receiving signals between a bilateral bus line and a serial-by-word data transmission line.

US 4,390,969 to Hayes discloses an asynchronous data transmission system with state variable memory and handshaking protocol circuits. The circuit is a stored state circuit including a memory and an output register with an input line and an input request line coupled to the memory and the output register having an output data line and an output acknowledge line.

US 4,426,697 to Petersen, et al. discloses a bus systems with address and status conductors. The address conductor carries mutually spaced serially binary coded bit patterns of m address bits, and the status conductor carries a serial bit pattern or r status bits.

US 4,433,413 to Fasang discloses a microprocessor system including a pseudo-random pattern generator, a signature register, supplemental control logic, serial and parallel I/O port test logic, and an LED display. Test instructions and the pattern generator provide test input data. The signature register and the microprocessor process the test results and present them on the display.

US 4,439,858 to Petersen discloses a digital in-circuit tester for high speed computer control in obtaining high pulse fidelity at each electrical node of a circuit under test. The tester includes a plurality of programmed memory digital test-signal generators responsive to the computer for generating and supplying to the nodes of the circuit under test a complex sequence of digital logic signals. High pulse fidelity is obtained by minimizing the current in the power supply and digital test signal loops.

US 4,441,075 to McMahon discloses the testing of individual chips and interchip connections on or within a high density packaging structure without a precision probe using Level Sensitive Scan Design rules. Basis for divisional patents US 4,494,066 and US 4,504,784.

US 4,483,002 to Groom, Jr., et al. discloses defining a display window for display of signals at selected test points. An operator defines signals at the beginning of the window and at the end of the window, but only after specified conditions. Corresponds to EP 0,093,229 and JP 58-190,784.

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US 4,484,329 to Slamka, et al. discloses the jaw contacts of a clip 10 connecting a device under test to the external interface block 14 of a test device. Signals from the device under test are compared with signals output from a library block 20.

US 4,488,259 to Mercy discloses Level Sensitive Scan Design strings on an integrated digital logic circuit to provide multiple functions of providing control parameters to logic blocks in the integrated circuit chip, and for providing reconfiguration messages to reconfiguration logic on the integrated circuit chip, in addition to the normal function of transferring test data to various portions of the integrated circuit chip. This reduces the number of input/output pads on the integrated circuit chip which must be dedicated to these functions.

US 4,493,077 to Agrawal et al. discloses LSI circuits including level sensitive mater latches and slave latches receiving two clock or control signals for normal mode operation. The conditions to initiate the scan testing mode are imposed on the standard clock terminals.

US 4,494,066 to Goel, et al. discloses chips in a module or any second level package. The test mechanism built into each chip will be used in place of mechanical probes to perform a chip-in-place test and interchip wiring test of the package. Level sensitive scan design rules need to be used for each chip and for the package clock distribution network. Divisional patent of US 4,441,075 and corresponds to US 4,504,784.

US 4,498,172 to Bhavsar discloses a built-in test system that employs a dual-mode feedback shift register to supply test vectors and evaluate test responses of functional and interface networks of a logic system. Test responses are supplied to a quotient bit compressor that generates a system response signature for comparison with an expected fault-free signature to producer a system pass/fail status signal.

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US 4,503,536 to Panzer discloses a digital unit testing system using signature analysis. Memory 10 provides test patterns and a memory 12 provides expected test signature patterns. The response data from the unit under test are converted into a signature in signature analyzer 20. Comparator 22 compares the outputs of signature analyzer 20 and memory 12. The test patterns are applied to the unit under test in step with clock 24 and sequential counter 26.

US 4,513,373 to Sheets discloses a local area network using protocol converters 30, 32, 34 and 36 to translate to a computer 52 with an incompatible communications format.

US 4,513,418 to Bardell, Jr. et al. discloses modifying and connecting together in series the LSSD scan paths on a number of logic circuit chips to simultaneously serve as a random signal generator and data compression circuit to perform random stimuli signature generation.

US 4,514,845 to Starr discloses locating a bus fault by placing devices in a high impedance state and sensing current flow between devices.

US 4,519,078 to Komonytsky discloses LSI and discrete logic circuits, including Level Sensitive Scan Design, that incorporate internally generated pseudorandom sequences as test vectors to stimulate the logic circuits under test. Responses to the test vectors are analyzed internally or externally using signature analysis to determine if the circuit has functioned properly.

US 4,534,028 to Trischler discloses applying a first digital test pattern to the primary inputs of a complex digital circuit while a second digital test pattern is shifted into a scan path of shift registers. The digits appearing at the primary outputs are repeatedly compared with those of a first digital number indicative of the proper operation of the circuit as each digit of the second digital test pattern is shifted into the scan path shift register.

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US 4,553,090 to Hatano et al. discloses a method of testing a logic circuit having a plurality of flip-flops associated with a scan path and combination circuits. The method: transforms parallel input data to serial input data, sets the serial input data in each selected flip-flop, performs a logic operation in the combination circuits on the data stored in the flip-flops, stores the resulting data in the flip-flops and outputs the output data in parallel.

US 4,575,674 to Bass, et al. discloses a diagnostic circuit for diagnosing a plurality of serially connected flip-flops in real time. See Figure 2.

US 4,577,318 to Whitacre, et al., discloses comparing A data on the 26 lines of data set A with B data on the 26 lines of data set B. The lines of A data and the lines of B data are fed to selector multiplexers 505a and 505b. The outputs of these multiplexers are fed to an EOR circuit 502 for comparison. A mask register 501 connects to the selector multiplexers in order to blank out selected input lines to multiplexers 505a,b. Mask register 501 has an input CI bus 501ci, which carries the bus control signals from bus control unit 510, which in turn connects to the D or data bus 34.

US 4,587,609 to Boudreau, et al. discloses a lockout circuit used in an asynchronous shared computer system. A first unit can lock a shareable unit to deny access to other units seeking to lock the shareable unit. Other units can access the shareable unit if they are not seeking to lock it.

US 4,594,711 to Thatte discloses a universal testing block (UTB) for on-chip testing of a VLSI subsystem such as a ROM or an ALU. The UTB can act as a test generator and a test evaluator.

US 4,597,042 to d'Angeac, et al. discloses a device for loading data in, and reading data out of a plurality of latch strings which are contained in a data processing system for testing, failure isolating and initializing. The device is operable to transmit test or initialization data to a plurality

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of latch strings in a system realized in accordance with the Level Sensitive Scan Design technique. In Figure 4, addressing unit Mi includes SRL latches 42, 43, and 44 providing three address bits that select one of eight strings. The three address bits are connected to string selector 48, which produces one of eight select signals 49-1 through 49-8.

US 4,597,080 to Thatte, et al. discloses a method and apparatus for testing VLSI processors using a bit-sliced bus-oriented data path including data and control monitors and BIT for the on-chip memory. The control monitor is used to decouple the testing task of the control section from that of the data path.

US 4,598,401 to Whelan discloses a signature analysis circuit. Responses to test patterns applied to the circuit under test are applied to a linear feedback signature register (LFSR). The LFSR produces a signature signal dependent upon its prior state and the responses. The outputs of the LFSR are applied as the address to a memory part having a 1 or 0 output, depending on whether the part tests true or fails. The checking occurs during the testing sequence, in contrast to conventional signature analysis testing where the analysis occurs only at the end of test.

US 4,601,034 to Sridhar discloses an apparatus for testing VLSI memory elements including a parallel signature analyzer.

US 4,602,210 to Fasang et al. discloses a plurality of scan paths in an IC fro testing. Each scan path includes plural bistable scan path flip-flops isolated from the combinational circuits.

US 4,612,499 to Andresen, et al. discloses a test input demultiplexing circuit in which a test signal is multiplexed with a data input line.

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US 4,615,029 to Hu, et al. discloses a ring transmission network for interfacing control functions between master and slave devices. A test/maintenance controller 120 interfaces with a slave device 96 through a serial transmission line 106.

US 4,618,956 to Horst discloses testing the inputs of an ALU to see if logical AND is zero or the two inputs are equal whiles allowing the ALU to perform another function at the time the tests are made. Corresponds to EP 0,136,174 and JP 60-168,243.

US 4,621,363 to Blum discloses including interface registers in the Level Sensitive Scan Design chain of shift registers. During testing, test data and response data are effected through the interface resisters to the system bus.

US 4,627,018 to Trost, et al. discloses a system to accelerate the granting of prioritized memory requests to a multiport memory system. The system detects one remaining request in the memory, and clears the priority logic before the requestor would normally be activated to receive the next group of memory requests.

US 4,628,511 to Stitzlein, et al. discloses recording pre- and post-failure events to analyze signal activity on an input/output channel to determine failing equipment.

US 4,635,193 to Moyer, et al. discloses a data processor having selective breakpoint capability communicates with a peripheral device to set the breakpoints. The instruction execution control means receive an operand from the peripheral device and selectively store the operand in the instruction register in response to the execution of a breakpoint instruction.

US 4,635,261 to Anderson, et al., discloses an on chip test system for configurable gate arrays with plural gates coupled to inputs and outputs of the chip. The gates may asynchronously receive signals from the inputs and asynchronously send signals to the outputs. In Figure 3, input

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shift registers 23 and output shift registers 25 are connected in series to provide test signals to the outputs of the circuit 20, to connect to further circuits through bond pad 36 and to provide self test of the shift registers themselves. In Figure 4, input registers 23 are connected together to form a pseudo-random pattern generator 30 with outputs connected to the gates 21. The output registers 25 are connected in series to form a signature analysis register 40 receiving the outputs from the gates 21.

US 4,638,313 to Sherwood, et al. discloses addressing for a multipoint communication system for patient monitoring.

US 4,642,561 to Groves, et al., discloses compressing the amount of data stored in local test data RAMs for implementing a circuit test.

US 4,646,298 to Laws, et al. discloses a computer system having intelligent and non-intelligent processing circuits that communicate with one another through connection slots of a communication bus. Each intelligent processing circuit has an identity memory and can specify in the memory that it performed and passed a self-test. The intelligent processing circuits that have passed the self-test arbitrate among themselves, based on their position on the communication bus, to determine which is to become the system test master to test the rest of the system and the non-intelligent processing circuits.

US 4,646,299 to Schinabeck, et al. discloses applying static analog voltages or currents to pins of a device under test and measuring resulting currents or voltages to evaluate the responses of the device being tested.

US 4,651,088 to Sawada discloses a logical and electrical characteristics tester having a measuring circuit corresponding to each pin on the device under test.

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US 4,669,061 to Bhavsar discloses a scannable flip-flop that can be used in testing combinational logic with test vectors.

US 4,672,307 to Bruer, et al. discloses testing combinatorial circuits by applying 1-transitions to the inputs. The accuracy of the outputs are checked by signature analysis or otherwise. An appropriate Gray code of 1-transistions are obtained from a ring counter and conventional counter.

US 4,674,089 to Poret, et al. discloses an in-circuit emulator (ICE). Capture logic 15 captures the contents of the program address register (PAR), the internal data bus (IDB), and various microprocessor 13 control (CONTROL) lines. The capture logic 15 provides outputs on lines 45 to trace circuits 25. Trace circuits 25 use a FIFO buffer to transfer the captured data to the output pins 31 of the chip 11. A content addressable memory 17 and a software programmable logic array 21 operate as a finite state machine to perform testing. The content addressable memory 17 determines the status of the processor and compares it with a set of four possible word recognizers with comparators 61. The content addressable memory 17 and software programmable logic array are apparently loaded from the microprocessor 13 over lines 41 through mode control 27 and lines 43.

US 4,679,192 to Vanbrabant discloses an arrangement for an orderly transmission of digital data between stations S1-Sn connected to a common communication path B. A main station distributes clock pulses on the communication path B. The clock pulses are counted in the stations S1-Sn. When the station number and the counting position agree, the relevant station is enabled to transmit data to one of the other stations.

US 4,680,539 to Tsai discloses a linear feedback shift register for inclusion in a level sensitive scan design (LSSD). A scan cell S4 includes a one bit register 23, see Figure 7, two

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exclusive NOR gates 19 and 20 and additional gates. Corresponds to EP 0,148,403 and JP 60-147,660.

US 4,680,733 to Duforestel, et al. discloses a device for serializing/deserializing bit configurations of variable length for loading and reading bit configurations in strings of latches.

US 4,683,569 to Rubin discloses connecting test points to shift registers that are read out bidirectionally. The data in the shift registers is shifted in each direction and compared to a reference data signal to indicate an error in a test point.

US 4,687,988 to Eichelberger, et al. discloses applying pseudo-random patterns in parallel to each of the inputs of an IC using LSSD design rules, forming an output signature and comparing the signature to a known good signature. Corresponds to US 4,745,355; and US 4,801,870.

US 4,694,293 to Sugiyama, et al. discloses a circuit used in an electronic musical instrument in which a number of musical tone generating circuits (receivers) are fed with different tone data by a single control circuit to produce different tones simultaneously.

US 4,698,588 to Hwang, et al. discloses a transparent shift register latch 170 for isolating peripheral ports during scan testing of a logic circuit. See Figure 8. The latch includes internal isolation gate 186. Corresponds to 5,032,783.

US 4,701,916 to Naven, et al. discloses an integrated circuit having plural registers. In operation, the registers act as parallel input/output registers. In a shift mode, the registers form a serial shift path and in a test mode, the registers act as a pseudo-random number generator and a signature analyzer.

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US 4,734,921 to Giangano, et al. discloses a fully programmable linear feedback shift register. A polynomial equation is first fed into the linear feedback shift register for setting the respective flip-flops into predetermined logic states, which are used to encode messages to be shifted by the programmable linear feedback shift register. Corresponds to WO 88/04097, EP 0,290,589, and JP 1-501,979.

US 4,740,970 to Burrows, et al. discloses a specific use of gates in a Built-In Logic Block Observation. Corresponds to EP 0,190,494 and JP 61-217,779.

US 4,743,841 to Takeuchi discloses a circuit selectively connecting an operative circuit or a test circuit to the bond pads of an integrated circuit.

US 4,752,929 to Kantz, et al. discloses testing a semiconductor memory part by subdividing the memory array into cell fields and comparing data bits in corresponding storage cells of each field.

US 4,759,019 to Bently, et al. discloses a programmable fault injection tool for testing a digital processing system. The tool injects faults for a user specified time duration and only after a user specified time delay.

US 4,763,066 to Yeung, et al. discloses comparing four digital test signals to known good reference signals. The four test signals are the result of analog horizontal and vertical signals directed to an integrator/A-D.

US 4,764,926 to Knight et al. discloses an integrated circuit having a built-in self test facility. The combinatorial logic is divided into sub-circuits A-F that are fed and observed by series connected registers flip-flops 1-8. See Figure 3. Multiplexers M4-M6 select the serial input to each

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register to include the output of down stream registers. See Figure 7. Corresponds to EP 0,195,164 and JP 61-155,878.

US 4,777,616 to Moore, et al. discloses a logic analyzer instrument that acquires digital samples from plural logic signals in a main frame computer and displays the edges of the signals enlarged and with precision.

US 4,783,785 to Hanta discloses diagnosis of logical circuits. Input latches 6 capture test data and apply it to combinatorial circuits 5. An output latch 7 captures the response data. Circuit 19 compares the response data to known good data. Corresponds to DE 3,700,251 A1 and JP 62-159,244.

US 4,788,683 to Hester, et al. discloses a converter between a system processor and a support processor for controlling testing of the system processor. A parallel-to-serial and serial-to-parallel converter conveys LSSD test signals between the two processors.

In Fig. 3A, debug logic includes an instruction address comparator 11 and an instruction op-code comparator 12. Select logic 13 determines which comparator output is selected. An instruction compare address register 14 and an op-code compare address register 16 are accessible by the LSSD scan strings on line 30a, and contain the desired instruction and op-code compare values, respectively. In addition to the selection between stop on instruction address or op-code made by the selection logic 13, stop enable logic 17 contains a single latch bit to enable the stop-on-address function.

One output is provided for the compare output 18 and a separate output is provided for the stop-on-address function 19. The compare output from 18 can be used as a sync pulse to an external logic analyzer. The stop output from 19 is used in conjunction with the external clock generator to disable the clocks when the stop address is detected. A third output 21 is provided

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which toggles each time an instruction is executed. This "Instruction Complete" output is required to implement an instruction single step function, since instructions may take more than one cycle to execute. (21 OCT 03)

US 4,791,358 to Sauerwald, et al. discloses a method of testing an interconnection between two integrated circuits which are mounted on a carrier and which are interconnected by data connections, for example a printed wiring board. The integrated circuits are also connected to an I^2C serial bus via which test patterns and result patterns can be communicated. Corresponds to US 4,879,717.

US 4,799,004 to Mori discloses a transfer circuit for operational test of LSI systems. Serial scan registers connected in series shift test data to the inputs of functional blocks 11 and 12 and serial scan registers capture the response data from the functional blocks and shift the response data out.

US 4,799,052 to Near, et al. discloses a method of determining access on an electronic serial bus by implicit token passing. Each device on the serial bus includes a bus access timer that carries a unique value for that device. Each bus access timer begins counting at an end of transmission signal on the bus and stops either when the count equals a unique count for that device or at a start of transmission signal on the bus.

US 4,800,418 to Natsui discloses an integrated circuit having a reference element selectively operated by an over-voltage applied to a bonding pad.

US 4,802,163 to Hirabayshi discloses a test facilitating circuit. Serially connected latches F1-F6 are interposed between modules M1-M3.

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US 4,808,844 to Ozaki, et al. discloses a bonding pad selection switch circuit connecting a bond pad to an internal circuit in response to a control signal applied to another bond pad.

US 4,811,299 to Miyazawa, et al. discloses a DRAM part that enters a test mode upon the combination of a column address strobe signal, a row address strobe signal and a write enable signal, which normally do not occur together. Corresponds to US 4,992,985; US 5,117,393, and JP 62-250,593.

US 4,812,678 to Abe discloses a through passage circuit selectively short-circuiting an input circuit to an output circuit. Corresponds to DE-A-3,709,032 and JP 62-220,879.

US 4,817,093 to Jacobs, et al. discloses testing a multi-chip packaged structure by isolating the one chip under test, applying test signals to that chip, creating a signature of the response signals from that chip and comparing the signature to that of a known good chip.

US 4,819,234 to Huber discloses a debugger, which performs several different functions including identifying and inserting breakpoints, that is part of the operating system of a processor with virtual memory.

US 4,821,269 to Jackson, et al. discloses a diagnostic system for a digital signal processor that monitors various internal test points within several modules. Any test point can be connected to a diagnostic bus for display from an output module.

US 4,825,439 to Sakashita, et al. discloses having an operating mode in which operational signals are output in parallel and a test mode in which serial input test signals can be output in parallel and the operational signals can be output as serial output response signals.

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US 4,833,395 to Sasaki, et al. discloses signal generators 11 and 12, input buffer 13 and output buffer 16 for testing a logic circuit 14.

US 4,833,676 to Koo discloses a method and apparatus for testing for stuck open faults in integrated circuits 10 having a plurality of combinational logic devices 18, 20. A chain of shift registers 22 each include latches L1 and L2 for holding respectively the detection test pattern and the initialization test pattern. See the scan cell of Figure 2.

US 4,855,954 to Turner, et al. discloses an in-system programmable device, using non-volatile programmable memory cells, that may be configured or re-configured while installed in a user's device. The normal device inputs and outputs are isolated during programming.

US 4,857,835 to Whetsel discloses a global event qualification system. The system provides the timing and control required to activate an IC's test logic during normal functional operation. The input and outputs of an IC are bordered by unique comparator cells or Event Qualifier Cells (EQCELL). The EQCELLs compare the data entering or leaving the IC to test data vectors loaded during a scan operation. The EQCELL generates a control signal when the comparison is true. Corresponds to EP 0,315,475.

A local controller 24 is used to control built-in test logic in logic core 22. The control lines necessary for this are indicated by bus 8. The local product terms 9 and 31 are ANDed by AND gate 30. This generates a global product term on bus 5. The global product term on bus 5 is fed back into the local controller 24. This allows the local controller to react to the occurrence of a global event. The local controller 24 will start the test of logic core 22 when bus 5 changes state.

US 4,860,288 to Teske, et al. discloses a test system including a ring oscillator distributed around the periphery of the VLSI chip and an I/O cell connected to each signal pin, from which are built the serially connected input registers and output registers. This provides a more accurate

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measurement of clock skew by providing a clock monitor pin directly connected to the clock bus internal to the VLSI chip. Corresponds to US 4,912,709.

US 4,860,290 to Daniels, et al. discloses a logic circuit having individually testable logic modules. Each of the modules may be selected for testing by means of a scan path in the module made up of serial register latches (SRLs) 34. Each module has a test port 28a.

US 4,862,071 to Sato, et al. discloses high speed circuit testing apparatus having plural test conditions. See Figure 10. Level comparison sections 300 receive an output from circuit under test and reference voltages H and L. The outputs of the level comparison sections 300 become the inputs to logical comparison sections 400. Each logical comparison section 400 includes signal detectors 402 and 403 respectively detecting the presence of the response signal using the strobe pulses STRB 1 and STRB 2.

US 4,862,072 to Harris, et al. discloses a set of four pins of an LSI chip providing access by a serial data line to macrocells or other partitioned logic of the LSI for individual test. The macrocells are connected to the remainder of the logic by a pair of multiplexer/test register combinations, one at the input and one at the output of the macrocell.

US 4,864,570 to Savaglio, et al. discloses a processing pulse control circuit for use in treating indeterminate signature increments in an apparatus producing RPT signature analysis of digital circuits. A memory stores clock count values where indeterminate signature increments will be encountered.

US 4,864,579 to Kishida, et al. discloses scan registers provided between circuit blocks.

US 4,866,508 to Eichelberger, et al. discloses, see Figure 4, loading test data into serial latches SR2A and SR2B, passing the test data through the circuits under test, such as latch 21c,

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counter 21b and "general" logic 21a, and capturing the resulting test data in serial scan latches
SR1A and SR1B.

US 4,870,345 to Tomioka, et al. discloses gate circuits 70-74 connected to the outputs of
scan registers 8-13 and 16 to control the input to the next circuit block, such as circuit block 36.

US 4,872,169 to Whetsel discloses a hierarchical scan selection system. A serial scan path
can be compressed or expanded to pass only through the desired logic element(s) to be tested.
Corresponds to JP 63-308,583.

US 4,875,003 to Burke discloses using a LSSD boundary scan chain to test input and output
cells of a circuit.

US 4,878,168 to Johnson, et al. discloses applying serial test information through a serial
bus to a storage control unit that interfaces a processor and a storage unit. The control unit changes
the serial data from the serial bus to parallel data normally provided by the processor. The test
information thus becomes indistinguishable from parallel data applied directly from the processor
along a parallel bus.

US 4,879,717 to Sauerwald, et al. corresponds to US 4,791,358.

US 4,887,262 to van Veldhuizen discloses a single-channel bus system for multi-master use
with bit cell synchronization, and master station comprising a bit cell synchronization element
suitable for this purpose.

US 4,887,267 to Kanuma discloses a logic circuit having a FIFO memory circuit to store
values from a test node. The FIFO memory then is unloaded to trace the outputs of such as the
states of an internal bus.

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US 4,893,072 to Matsumoto, et al., discloses testing an IC device 21 that includes a logic circuit section L and a memory circuit section M. Logic circuit section L includes flip-flops 30, 31, 32, and 33 that provide time delays between input and output signals through the IC 21. An IC-device testing apparatus 23 includes flip-flop circuits F11, F21, F22, ..., Fnn, that provide for matching the time delays through the logic circuit section L of actual test signals applied to the IC 21 and expected signals EX. The IC tester applies a test signal to an IC under test and an expected response signal to the input of a shift register. The shift register is clocked to produce the expected response signal at its output at the same time the IC should produce its response to the test signal. The tester then compares the expected response signal to the actual response signal.

US 4,894,830 to Kawai discloses an LSI chip with scanning circuitry for generating reversals along activated logical paths. A pulse is scanned along first flip-flop circuits to propagate test signals through the activated logical paths. A second string of flip-flops connect to the outputs of the logical circuits and are configured into a linear feedback shift register to determine the dynamic performance of the logic circuit.

US 4,896,262 to Wayama, et al. discloses a memory system having a semiconductor memory providing faster access than a magnetic disk storage system.

US 4,897,842 to Herz, et al. discloses a signature generator connected to plural circuit nodes to be tested.

US 4,899,273 to Omoda, et al. discloses a clock-synchronized simulation method of simulating the logic operations of combination circuits between flip-flops, while operating the flip-flops at a constant time, by using clock signals as conditions for setting and resetting the flip-flops.

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US 4,903,266 to Hack discloses a system and method for on-chip self test of memory circuits. The testing includes a random pattern generator addressing all memory locations and using a linear feedback shift register to generate a signature of the test results. A level sensitive scan design serial bus can test all logic and the combination can provide a final test signature.

US 4,907,230 to Heller, et al. discloses a device comparing the digital or analog outputs of circuit boards or other units under test with known good models. A clip connects each point of the circuit under test to a pin of the test instrumentation.

US 4,910,735 to Yamashita discloses an integrated circuit having plural logic blocks. Each logic block has an operational circuit, a pattern generator, and a switching circuit for selecting either an operational input signal or the pattern signal as the input to the operational circuit. Corresponds to EP 0,273,821 and JP 63-153,483.

US 4,912,633 to Schweizer, et al. discloses an hierarchical multiple bus computer system including a master bus and slave buses, which master and slave buses are substantially identical. Communication between the master bus and a slave bus is effected through a combination of an interface controller 12, a shared dual port RAM 14 and a shared RAM controller 13.

US 4,912,709 to Teske, et al. corresponds to US 4,860,288.

US 4,918,379 to Jongpier discloses providing an integrated circuit with macro circuits that can be individually tested. A test bus extends along the integrated circuit and connects with a test interface circuit in each macro circuit. The test interface circuits are connected in series.

US 4,924,468 to Horak, et al. discloses a logic analyzer measuring signals that are delivered by a number of targets, such as microprocessors, that are not correlated in time.

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US 4,926,425 to Hedtke, et al. discloses a system for testing successive component groups separated by accessible nodes. The process observes data at the nodes and supplies test data to the nodes.

US 4,929,889 to Seiler, et al. discloses a test/load bus internal to an integrated circuit to supply test data to test nodes internal of the chip and unload response data from the test nodes.

US 4,930,216 to Nelson discloses a process for preparing integrated circuit dies, while still in wafer form, for surface mounting direct to a substrate without requiring packaging of the dies and maintaining corrosion resistance.

US 4,931,722 to Stoica discloses serial scan paths of registers for serially scanning test data into and out of the registers, applying the serial test data in parallel to combinational logic between the paths and receiving parallel test result data from the combinational logic.

US 4,931,723 to Jeffrey, et al. discloses a test device having plural tester channels. Each channel has a channel control circuit means coupled to a pin of a unit under test for controlling the state of operation of the pin.

US 4,935,868 to DuLac discloses an integrated circuit for interfacing a standard IEEE 796 bus to a VSB-type buffer bus. the circuit includes a DMA channel for high speed access of the IEEE 796 to the buffer bus and a slave bus channel for high speed access of the buffer bus to the IEEE 796 bus. A third bus interface connects to a local processor to assist in arbitration and control during some types of data transfers.

US 4,937,826 to Gheewala, et al. discloses pre-charging sense lines to known signal levels immediately prior to using the sense lines to sense the signal level at a test point. This eliminates the need for sequential patterns to detect "stuck-open" faults.

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US 4,943,966 to Guinta, et al. discloses a serial diagnostic bus (SDB) connecting to a memory control unit. Over the SDB, the system console 30 can read from and write to registers in memory boards 12 and 14.

US 4,945,536 to Hancu discloses connecting input and output signals to a boundary scan register, using three types of boundary scan cells 230, 240 and 250.

US 4,947,106 to Chism discloses a test module testing an analog to digital converter by deterministically checking higher order bits and non-deterministically checking lower order bits.

US 4,947,357 to Stewart, et al. discloses a circuit board carrying plural integrated circuits, each with an internal scan chain. The scan input of each integrated circuit is connected to a system scan controller 26. The scan outputs of the integrated circuits are connected to multiplexer 30 for selective testing of individual integrated circuits.

US 4,956,602 to Parrish discloses wafer scale testing of redundant integrated circuit dies. In Figure 2, wafer test pads 14 are selectively connected by input/output buffer circuit 16 to dies 12 to carry test signals to the dies and carry response signals back to the test pads. Corresponds to US 5,053,700.

US 4,961,053 to Krug discloses arranging test circuits on a wafer, the wafer also carrying the integrated circuits to be tested. Power is applied to the wafer and testing occurs automatically.

US 4,969,121 to Chan, et al. discloses an integrated circuit programmable logic array circuit with improved microprocessor connectability.

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US 4,974,192 to Face, et al. discloses a communications processor 46 for a personal computer. Corresponds to WO-A-89 01,202.

US 4,974,226 to Fujimori, et al. discloses comparing data stored in a data register 13a with a 1 bit signal stored in a scan latch 1c to determin coincidence or non-coincidence therebetween.

US 4,989,209 to Littlebury et al. discloses an interface apparatus for coupling a multi-channel tester to high pin count integrated circuits. Test stimulus data is applied in parallel to circuits 21 through shift registers 16 and 18. Test response data is assembled in register 17 and returned to tester 11.

US 4,992,985 to Miyazawa, et al. corresponds to US 4,811,299.

US 5,001,713 to Whetsel discloses an event qualification testing architecture. A boundary test architecture uses input and output test registers 12, 22 having functions controlled by an event qualifying module (EQM) 30. In response to the EQM receiving a matching condition signal from the register 22, the EQM may control the test registers 12, 22 to perform a variety of tests on the incoming and outgoing data. The internal functional logic 20 may continue to operate at speed during the testing to determine faults not otherwise discoverable. Corresponds to US 5,103,450; EP 0,382,360, and JP 3 020,683.

US 5,008,885 to Huang, et al. discloses inserting errors into parts at controlled times through programmable masks.

US 5,014,186 to Chisholm discloses a data processing system having a bus system coupling I/O units to a storage unit. The I/O units are supplied a line size signal representing the line size of the storage unit. The I/O units respond to this line size signal to adjust the data transfer size or packet of the I/O unit to match the storage unit line size.

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US 5,023,872 to Annamalai discloses simple error detection logic with an error counter and a timer detects errors in a dual token ring network.

US 5,042,005 to Miller, et al. discloses a timer circuit with match recognition features.

US 5,051,996 to Bergeson, et al. discloses a built-in test by signature system that provides fault detection by the bits in the signature detection logic.

US 5,053,949 to Allison, et al. discloses a debug peripheral that uses externally provided instructions to control a core processing unit.

US 5,054,024 to Whetsel discloses a system scan path architecture, provided by a device select module (DSM) 18. The DSM selects secondary scan paths (PATH1-m) on each circuit for coupling with a primary scan path on a test bus 14. Remote bus masters 124 may be used in conjunction with the DSMs to provide serial-scan testing independent of the primary bus master 12. Corresponds to 5,056,093.

US 5,056,094 to Whetsel discloses a delay fault testing system. A special test instruction to a boundary test cell invokes a toggle mode that allows the output boundary of an IC to output a transition between logic states on the edges of a clock signal. The same test instruction configures a boundary test cell of a receiving IC to sample input data on the subsequent edge of the clock signal. The sampled data can be inspected to determine whether the output signal propagated to the receiving IC in the prescribed time.

US 5,077,740 to Kanuma discloses testing individual macrocells of a logic circuit by shifting test data into register 12, shutting off an input path for normal operation signals to the macrocell, and applying the test data in register 12 to the macrocell. An output register 14 receives

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the output of the macrocell under test and the contents of register 14 is shifted out, while shutting off an output path of normal operating signals from the macrocell.

US 5,084,814 to Vaglica, et al. discloses a CPU having access to on-chip and off-chip peripherals and memory in both a normal and alternate mode of operation by means of a parallel bus, which it operates as a bus master. In an alternate mode, the CPU receives instructions on a serial bus on which the CPU is a slave device.

US 5,084,874 to Whetsel discloses a testing buffer register 12. See Figure 2. The test cell can also include compare and other logic. See Figures 6 and following. Corresponds to US 5,495,487; US 5,602,855; US 5,631,911; US 6,081,916; US 6,304,987; and US 6,611,934.

US 5,090,015 to Dabbish, et al. discloses a self checking electronically erasable programmable array logic. The device verifies the storage integrity of each cell within the array during programming, after completing programming, and prior to executing the algorithm stored in the array.

US 5,103,450 to Whetsel discloses a set of event qualified test protocols for use in testing integrated circuits. A boundary scan architecture for use in the integrated circuit (10) comprises input and output test registers (12,22) having functions controlled by an event qualifying module (EQM) (30). The EQM (30) receives a signal indicating a matching condition has been met. The EQM receives additional signals which indicate which testing protocol of the possible protocols is selected. The EQM (30) may control the input and output test registers (12,22) to perform a variety of tests on the incoming and outgoing data. During testing, the internal logic (20) may continue to operate at speed, thereby allowing the test circuitry to detect faults which would not otherwise be observable. A memory buffer (64) may be included to store a plurality of input data for test data. A set of standard protocols allow interoperability between EQMs on multiple IC's in a circuit. By adhering to a standard set of standard event qualification protocols, all IC designs

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produced with the boundary scan architecture will be capable of operating together to perform advanced test operations of the circuit is response to a condition.

US 5,109,383 to Chujo discloses scan path latch circuits. The latch circuits include three switches and two flip-flops

US 5,128,664 to Bishop discloses a search technique for identifying slave devices connected to a serial bus. When a master controller senses a condition that requires a condition that requires an assessment of devices on the bus, it examines the addresses of previously connected devices at more frequent time intervals than it does for addresses that were not previously associated with connected devices.

US 5,133,062 to Joshi, et al., discloses a RAM buffer controller for providing simulated first-in first-out (FIFO) buffers in a random access memory.

US 5,155,432 to Mahoney discloses a system for scan testing of logic circuit networks. Switching means are selectively varied to provide different test circuit configurations for different modes of operation.

US 5,159,465 to Maemura, et al. discloses a facsimile machine having a transmission speed selective downshift function. A common buffer memory provides for temporarily storing coded image information either in an Error Correction Mode or a normal transmission mode.

US 5,161,160 to Yaguchi, et al. discloses scan paths SP100-SP107 connected to different bus lines IB0-IB7, respectively.

US 5,167,020 to Kahn, et al. discloses a serial data transmitter with dual buffers operating separately and having scan and self test modes.

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US 5,170,398 to Fujieda, et al., discloses a test pattern generating device for a memory having a logical operation function. The device uses a pattern generator and a tester CPU to generate address and data that are compared to the output of a device under test.

US 5,173,906 to Dreibelbis, et al., discloses a built-in self test for integrated circuits. A deterministic data pattern generator is provided on the VLSI chip, and operates to test a chip module and provide a fail/no-fail result, along with data identifying where the fail occurred.

US 5,187,795 to Balmforth, et al. discloses a pipelined signal processor having plural bi-directional configurable parallel ports that are configurable as individual ports or as coupled pairs of ports.

US 5,214,760 to Hammond, et al. discloses an adaptable multi-port data buffer.

US 5,218,702 to Kirtland discloses a system for selecting request for a resource before decoding of requested resource address and validating selection thereof.

US 5,276,807 to Kodama, et al. discloses bus interface synchronization circuitry for reducing time between successive data transmission in a system using an asynchronous handshake.

US 5,303,148 to Mattson discloses a voice recognition system for doctors in surgery. The machine compares received audio to stored known words and displays the words on a screen.

US 5,329,471 to Swoboda et al. discloses an emulation system using state machines for a microprocessor. The system provides emulation, simulation and testability without physical probing or special test fixtures. The system provides a serial scan testability interface having first and second scan paths. The first scan path is provided for applying digital information to the

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functional circuit for use in emulation of the functional circuit. The second scan path connects to state machine circuits that have a sequence of states responsive to the emulation command codes. The disclosed system also incorporates a JTAG interface and has different clock signal domains. Corresponds to US 4,860,290 and US 6,522,985.

US 5,495,487 to Whetsel corresponds to US 5,084,874.

US 5,535,331 to Swoboda, et al., discloses that operations of a data processing device are traced by detecting a jump address in the program counter sequence, and pushing the jump address onto a trace stack. Corresponds to US 5,109,494; US 5,101,498; US 5,072,418; US 5,142,677; and US 5,155,812.

US 5,623,500 to Whetsel corresponds to US 5,353,308.

US 5,958,072 to Jacobs, et al., discloses test-event hardware that can be repeatedly generated during a test procedure without repeated intervention by a test program. The hardware is located in the processor to memory bus interfaces of a system having multiprocessors.

US 6,457,148 to Yoshiba discloses testing an IC 2 with test units 4-1 and 4-2. To test a synchronous IC, pattern delay circuits 6-1 set a time delay corresponding to the latency set in the IC 2. The pattern delay circuits are connected between a pattern generator 10-2 and a logical comparator 9-2.

US 6,601,193 to Liebau discloses an event recognition unit for recognizing and/or monitoring events on an information bus. A comparator provides a sequencer signal to a state machine when a pattern on the bus matches a pattern term of the comparator. The state machine provides the pattern term to the comparator.

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US Patent Application Publications

US 2001/0049803 to Kurafuji discloses a microprocessor internally provided with a test circuit. The test circuit includes a test event signal output terminal and an external event request signal input terminal.

US 2002/0133774 to Inoue discloses an expected data generating unit and a determination unit that compares the measurement result data.

US 2002/0194565 to Arabi discloses simultaneously testing N identical integrated circuit blocks. Each block contains M scan chains. The I th scan chains in each block are identical. A test vector is simultaneously applied to each block's I th scan chain and the resulting outputs are compared. If the outputs are equal, the chain is defect free for all N blocks.

US 2002/0199143 to Alt, et al., discloses testing circuit modules.

US 2003/0005379 to Slawecki, et al., discloses a comparison circuit and method for verification of scan data.

US 2003/0014704 to Nishimura discloses a tester supplying data signals, clock signals, and expected value data to a self-test circuit on a semiconductor device.

US 2003/0033556 to West discloses a test system formatter configurable to operate in any one of a plurality of drive modes.

US 2003/0140295 to Antley, et al., discloses test circuitry selectively connected to the functional circuits during testing. After testing, the test circuits are electrically isolated from the

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functional circuits and power supplies so they do not load the functional circuit or consume power.

Foreign Patent Document

JP 63-198,884 discloses scan paths 10 and 20 connected in series. Clocks are supplied to each scan path independently from clock input terminals 6a and 6b. Only a necessary scan path isput in operation at the time of test, so data for the test are set and taken out of the scan path without any unnecessary shift operation and the test time is shortened.

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				TI-14124D.6		10/691,225	

LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)

APPLICANT
Lee D. Whetsel

FILING DATE	GROUP
10/22/2003	2133

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		3,633,100	1/4/1972	Heilweil, et al.	324	73	5/12/1970
		3,651,315	3/21/1972	Collins	235	151.31	4/29/1970
		3,657,527	4/18/1972	Kassabgi, et al.	235	153	10/16/1969
		3,723,868	3/27/1973	Foster	324	73 AT	1/21/1972
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		4,268,902	5/19/1981	Berglund, et al.	364	200	10/23/1978
		4,286,173	8/25/1981	Oka, et al.	307	440	3/27/1978
		4,308,616	12/29/1981	Timoc	371	23	5/29/1979
		4,309,767	1/5/1982	Andow, et al.	371	24	8/21/1979
		4,312,066	1/19/1982	Bantz, et al.	371	16	12/28/1979
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		4,357,703	11/2/1982	Van Brunt	371	15	10/9/1980
		4,365,334	12/21/1982	Smith, et al.	371	27	2/9/1981
		4,366,478	12/28/1982	Masuda, et al.	340	825	1/5/1981
		4,390,969	6/1/1983	Hayes	395	550	4/21/1980
		4,426,697	1/1/1984	Petersen, et al.	340	825.52	1/24/1981

EXAMINER	DATE CONSIDERED

+EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. TI-14124D.6	SERIAL NO. 10/691,225

LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)

APPLICANT Lee D. Whetsel	
FILING DATE 10/22/2003	GROUP 2133

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		4,484,329	11/20/1984	Slamka, et al.	371	25	8/10/1981
		4,488,259	12/11/1984	Mercy	364	900	10/29/1982
		4,493,077	1/8/1985	Agrawal, et al.	371	25	9/9/1982
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		4,513,373	4/1/1985	Sheets	364	200	12/28/1982
		4,513,418	4/23/1985	Bardell, Jr, et al.	371	25	11/8/1982
		4,514,845	4/30/1985	Starr	371	15	8/23/1982
		4,519,078	5/21/1985	Komonytshy	371	25	9/29/1982
		4,534,028	8/6/1985	Trischler	371	25	12/1/1983
		4,553,090	11/12/1985	Hatano, et al.	324	73 AT	7/23/1980
		4,575,674	3/11/1986	Bass, et al.	324	73 R	7/1/1983
		4,577,318	3/18/1986	Whitacre, et al.	371	1	11/14/1983
		4,587,609	5/1/1986	Boudreau, et al.	395	726	7/1/1983
		4,594,711	6/10/1986	Thatte	371	25	11/10/1983
		4,597,042	6/24/1986	d'Angeac	364	200	9/13/1983
		4,597,080	6/24/1986	Thatte, et al.	371	25	11/14/1983
		4,598,401	7/1/1986	Whelan	371	25	6/25/1984
		4,601,034	7/15/1986	Sridhar	371	25	3/30/1984
		4,602,210	7/22/1986	Fasang, et al.	324	73	12/28/1984
		4,612,499	9/16/1986	Andresen, et al.	324	73 R	11/7/1983
		4,615,029	9/30/1986	Hu, et al.	370	89	12/3/1984
		4,618,956	10/21/1986	Horst	371	68	9/29/1983
		4,621,363	11/4/1986	Blum	371	25	12/6/1984
		4,627,018	12/1/1986	Trost, et al.	395	476	9/8/1983
		4,628,511	12/9/1986	Stitzlein, et al.	371	22	2/25/1982
		4,635,193	1/8/1987	Moyer, et al.	364	200	6/27/1984
		4,635,261	1/6/1987	Anderson, et al.	371	25	1/26/1985

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+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,638,313	1/20/1987	Sherwood, et al.	340	825.52	11/8/1984
		4,646,298	2/1/1987	Laws, et al.	371	16	5/1/1984
		4,642,561	2/10/1987	Groves, et al.	324	73 R	6/13/1983
		4,646,299	2/24/1987	Schinabeck, et al.	371	20	8/1/1983
		4,651,088	3/17/1987	Sawada	324	73R	5/6/1985
		4,669,061	5/26/1987	Bhavsar	365	154	12/21/1984
		4,672,307	6/9/1987	Breuer, et al.	324	73 R	12/20/1985
		4,674,089	6/16/1987	Poret, et al.	371	25	4/16/1985
		4,679,192	7/1/1987	Vanbrabant	340	825.52	1/24/1986
		4,680,539	7/14/1987	Tsai	324	73	12/30/1983
		4,680,733	7/14/1987	Duforestel	364	900	10/29/1984
		4,683,569	7/28/1987	Rubin	371	25	10/21/1985
		4,687,988	8/18/1987	Eichelberger, et al.	324	73 AT	6/24/1985
		4,694,293	9/15/1987	Sugiyama, et al.	340	825.68	9/16/1985
		4,698,588	10/6/1987	Hwang, et al.	324	73 R	10/23/1985
		4,701,916	10/20/1987	Naven, et al.	371	15	3/17/1986
		4,701,920	10/20/1987	Resnick, et al.	371	25	11/8/1985
		4,701,921	10/20/1987	Powell, et al.	371	25	10/23/1985
		4,710,931	12/1/1987	Bellay, et al.	371	25	10/23/1985
		4,710,932	12/1/1987	Hiroshi	371	25	1/15/1986
		4,710,933	12/1/1987	Powell, et al.	371	25	10/23/1985
		4,734,921	3/29/1988	Giangano, et al.	377	72	11/25/1986
		4,740,970	4/26/1988	Burrows, et al.	371	15	12/11/1985
		4,743,841	5/10/1988	Takeuchi	324	73 R	5/20/1985
		4,752,929	6/21/1988	Kantz, et al.	371	21	3/25/1986
		4,759,019	7/19/1988	Bentley, et al.	371	3	7/10/1986
		4,763,066	8/9/1988	Yeung, et al.	324	73R	7/23/1986
		4,764,926	8/16/1988	Knight, et al.	371	25	12/11/1985
		4,777,616	10/11/1988	Moore, et al.	364	900	5/12/1986
		4,783,785	11/8/1988	Hanta	371	25	1/5/1987
		4,788,683	11/29/1988	Hester, et al.	371	20	1/14/1986
		4,791,358	12/13/1988	Sauerwald, et al.	324	73 R	9/2/1986
		4,799,052	1/1/1989	Near, et al.	340	825.52	1/13/1986
		4,799,004	1/17/1989	Mori	324	73 R	1/25/1988

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+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,800,418	1/24/1989	Natsui	357	68	9/6/1984
		4,802,163	1/31/1989	Hirabayshi	371	15	12/29/1986
		4,808,844	2/28/1989	Ozaki, et al.	307	243	4/17/1986
		4,811,299	3/7/1989	Miyazawa, et al.	365	201	4/22/1987
		4,812,678	3/14/1989	Abe	307	443	3/23/1987
		4,817,093	3/28/1989	Jacobs, et al.	371	25	6/18/1987
		4,819,234	4/4/1989	Huber	371	19	5/1/1987
		4,821,269	4/11/1989	Jackson, et al.	371	16	10/23/1986
		4,825,439	4/25/1989	Sakashita, et al.	371	15	8/18/1987
		4,833,395	5/23/1989	Sasaki, et al.	324	73 R	10/23/1987
		4,833,676	5/23/1989	Koo	371	15	7/30/1987
		4,855,954	8/8/1989	Turner, et al.	365	185	3/4/1985
		4,857,835	8/15/1989	Whetsel	324	73	11/5/1987
		4,860,288	8/22/1989	Teske, et al.	371	1	10/23/1987
		4,860,290	8/22/1989	Daniels, et al.	371	25	6/2/1987
		4,862,071	8/29/1989	Sato, et al.	324	73 R	11/18/1988
		4,862,072	8/29/1989	Harris, et al.	324	73 R	9/8/1988
		4,864,570	9/5/1989	Savaglio, et al.	371	22.4	6/29/1987
		4,864,579	9/5/1989	Kishida, et al.	371	22.3	8/3/1987
		4,866,508	9/12/1989	Eichelberger, et al.	357	74	9/26/1986
		4,870,345	9/26/1989	Tomioka, et al.	371	22.3	8/3/1987
		4,872,169	10/3/1989	Whetsel	371	22.3	3/6/1987
		4,875,003	10/17/1989	Burke	324	73 R	2/21/1989
		4,878,168	10/31/1989	Johnson, et al.	364	200	10/29/1986
		4,879,717	11/7/1989	Sauerwald, et al.	371	22.3	9/2/1986
		4,887,262	12/12/1989	van Veldhuizen	370	85.1	3/15/1988
		4,887,267	12/12/1989	Kanuma	371	22.3	12/28/1987
		4,893,072	1/9/1990	Matsumoto	371	223	6/22/1988
		4,894,830	1/16/1990	Kawai	371	22.3	1/19/1988
		4,896,262	1/23/1990	Wayama, et al.	364	200	2/22/1985
		4,897,842	1/30/1990	Herz, et al.	371	22.4	11/5/1987
		4,899,273	2/6/1990	Omoda, et al.	364	200	12/10/1986
		4,903,266	2/20/1990	Hack	371	21.2	4/29/1988

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		4,907,230	3/6/1990	Heller, et al.	371	22.1	2/29/1988
		4,910,735	3/20/1990	Yamashita	371	22.4	12/17/1987
		4,912,633	3/27/1990	Schweizer, et al	364	200	10/24/1988
		4,912,709	3/27/1990	Teske, et al.	371	22.1	10/23/1987
		4,918,379	4/17/1990	Jongepier	324	73.1	8/31/1988
		4,924,468	5/8/1990	Horak, et al.	371	22.1	11/16/1988
		4,926,425	5/15/1990	Hedtke, et al.	371	22.6	6/9/1988
		4,929,889	5/29/1990	Seiler, et al.	371	22.3	6/13/1988
		4,935,868	6/1/1990	DuLac	364	200	11/28/1988
		4,930,216	6/5/1990	Nelson	29	854	3/10/1989
		4,931,722	6/5/1990	Stolca	371	22.5	11/7/1985
		4,931,723	6/5/1990	Jeffrey, et al.	371	22.3	12/18/1985
		4,937,826	6/26/1990	Gheewala, et al.	371	22.1	9/9/1988
		4,943,966	7/24/1990	Giunta, et al.	371	11.1	4/8/1988
		4,945,536	7/31/1990	Hancu	371	22.3	9/9/1988
		4,947,106	8/7/1990	Chism	324	73.1	3/31/1988
		4,947,357	8/7/1990	Stewart, et al.	371	22.3	2/24/1988
		4,956,602	9/11/1990	Parrish	324	158 R	2/14/1989
		4,961,053	10/2/1990	Krug	324	158 R	7/24/1985
		4,969,121	11/6/1990	Chan, et al.	364	900	3/2/1987
		4,974,192	11/27/1990	Face, et al	364	900	7/23/1987
		4,974,226	11/27/1990	Fujimori, et al.	371	22.3	9/22/1988
		4,989,209	1/29/1991	Littlebury, et al.	371	22.1	3/24/1989
		4,992,985	2/12/1991	Miyazawa, et al.	365	201	4/22/1987
		5,001,713	3/19/1991	Whetsel	371	22.3	2/8/1989
		5,008,885	4/16/1991	Huang, et al.	371	3	12/29/1988
		5,014,186	5/1/1991	Chisholm	395	850	8/1/1986
		5,023,872	6/11/1991	Annamalai	371	5.1	3/25/1988
		5,042,005	8/20/1991	Miller, et al.	364	900	8/19/1988
		5,051,996	9/24/1991	Bergeson, et al.	371	22.4	3/27/1989
		5,053,949	10/1/1991	Allison, et al.	364	200	4/3/1989
		5,054,024	10/1/1991	Whetsel	371	22.3	8/9/1989

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		5,056,094	10/8/1991	Whetsel	371	25.1	6/9/1989
		5,077,740	12/31/1991	Kanuma	371	22.3	1/30/1989
		5,084,814	1/28/1992	Vaglica, et al.	395	325	10/30/1987
		5,084,874	1/28/1992	Whetsel	371	22.3	9/7/1988
		5,090,015	2/18/1992	Dabbish, et al.	371	22.5	2/6/1989
		5,103,450	4/7/1992	Whetsel	714	724	2/8/1989
		5,109,383	4/28/1992	Chujo	371	22.3	9/1/1989
		5,128,664	7/1/1992	Bishop	340	825.52	5/5/1986
		5,133,062	7/1/1992	Joshi, et al.	395	500	3/6/1986
		5,159,465	10/1/1992	Maemura, et al.	326	73	10/5/1988
		5,155,432	10/13/1992	Mahoney	324	158 R	10/7/1987
		5,161,160	11/3/1992	Yaguchi, et al.	371	22.3	2/1/1990
		5,167,020	11/24/1992	Kahn, et al.	395	250	5/25/1989
		5,170,398	12/8/1992	Fujieda, et al.	371	27	7/18/1990
		5,173,906	12/22/1992	Dreibelbis, et al.	371	22.5	8/31/1990
		5,187,795	2/1/1993	Balmforth, et al.	395	800	1/27/1989
		5,214,760	5/1/1993	Hammond, et al.	395	250	8/26/1988
		5,218,702	6/1/1993	Kirtland	395	298	7/6/1988
		5,276,807	1/1/1994	Kodoma, et al.	395	309	4/13/1987
		5,303,148	4/12/1994	Mattson, et al.	364	413.01	11/27/1987
		5,329,471	7/12/1994	Swoboda, et al.	364	578	6/2/1987
		5,495,487	2/27/1996	Whetsel	714	736	9/7/1988
		5,329,471	7/9/1996	Swoboda, et al.	714	28	5/4/1989
		5,623,500	4/22/1997	Whetsel	371	22.1	8/6/1990
		5,958,072	9/28/1999	Jacobs, et al.	714	30	1/13/1997
		6,457,148	9/24/2002	Yoshiba	714	718	2/9/1999
		6,601,193	7/29/2003	Liebau	714	39	8/3/2000

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		2001/0014959 A1	8/16/2001	Whetsel	714	724	3/27/1997
		2001/0049803 A1	12/6/2001	Kurafuji	714	30	2/20/2001
		2002/0133774 A1	9/19/2002	Inoue	714	736	11/9/2001
		2002/0194565 A1	12/19/2002	Arabi	714	729	6/18/2001
		2002/0199143 A1	12/26/2002	Alt, et al.	714	726	3/15/2002
		2003/0005379 A1	1/2/2003	Slawecki, et al.	714	726	6/28/2001
		2003/0014704 A1	1/16/2003	Nishimura	714	736	3/18/2002
		2003/0033556 A1	2/13/2003	West	714	25	3/18/2002
		2003/0140295 A1	7/24/2003	Antley, et al.	714	733	1/18/2002

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
		JP 63-198,884	8/17/1988	Japan	G01R	31/28	X

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